UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/536,828	05/27/2005	Makoto Kitabatake	071971-0251	6640

20277 7590 10/27/2009

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
10/27/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/536,828	KITABATAKE ET AL.	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,12-15 and 17-19* is/are pending in the application.

4a) Of the above claim(s) *5,6 and 12-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,15 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/28/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. **Claims 15 and 17** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claim 15, the specification does not describe any embodiment wherein "another heat conducting member is in direct contact with lowest surface of said semiconductor chip," as recited in lines 2-3 of claim 15, **and** wherein "an area where the second intermediate member touches the lower surface of the semiconductor chip is larger than an area where the first intermediate member touches the lower surface of the semiconductor chip," as recited in lines 22-24 of claim 1.

Regarding claim 17, the specification does not describe any embodiment wherein "another semiconductor chip that is stacked on said semiconductor chip and a part of which connected to said first base material," as recited in lines 2-3 of claim 15, **and** wherein "an area where the second intermediate member touches the lower surface of the semiconductor chip is larger than an area where the first intermediate member touches the lower surface of the semiconductor chip," as recited in lines 22-24 of claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. **Claims 1-3, 15 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yanagisawa (US 2004/0080028)** in view of **Tamaki et al. (US 6,157,080; hereinafter, Tamaki)**.

With respect to **claim 1, Yanagisawa** teaches a semiconductor apparatus **(Fig. 2)** comprising:

a semiconductor chip **(11, Fig. 2)** including a power semiconductor device **(¶ [0005], [0038])**;

a first base material **(13, Fig. 2)** made of an electrically conductive material **(¶ [0040])** and electrically connected **(¶ [0038]: electrode 11b)** to a part of a lower surface of said semiconductor chip **(11)**;

a heat conducting member **(15, Fig. 2)** coming in contact with a part of an upper surface of said semiconductor chip **(11)** and releasing heat directly from said semiconductor chip **(¶ [0044])**;

an encapsulating material **(21, Fig. 2)** for encapsulating said semiconductor chip **(11)** and said heat conducting member **(15)**;

wherein the semiconductor apparatus further comprises a second base material **(14, Fig. 2)** made of a metal material **(¶ [0039])** and disposed on a part of said upper surface of said semiconductor chip **(11)**,

wherein said power semiconductor device is a vertical element **(¶ [0038])**,

wherein a part of said first base material **(19, Fig. 2)** is extruded outside said encapsulating material **(21)** and works as a first external connection terminal **(¶ [0038])**;

wherein a part of said second base material **(20, Fig. 2)** is extruded outside said encapsulating material **(9)** and works as a second external connection terminal **(¶ [0038])**,

wherein a first intermediate member **(11b, Fig. 2)** made of an electrically conductive material **(¶ [0038]: electrode)** is provided under the lower surface of said semiconductor chip and between said first base material **(13)** and said semiconductor chip **(11)**; and

wherein the semiconductor chip **(11, Fig. 3)** and the first base material **(13)** are electrically connected with each other through the first intermediate member **(11b, ¶ [0038])**.

Thus, **Yanagisawa** teaches all the limitations of the claim with the exception of disclosing:

a second intermediate member made of a material having a lower heat conductivity than said first intermediate member is provided under the lower surface of

said semiconductor chip and between said first base material and said semiconductor chip;

wherein the second intermediate member touches the lower surface of the semiconductor chip and the first base material, and area where the second intermediate member touches the lower surface of the semiconductor chip is larger than an area where the first intermediate member touches the lower surface of the semiconductor chip; and

wherein the power semiconductor device is constructed by using a wide band gap semiconductor.

However, **Tamaki** teaches a semiconductor device **(Fig. 1)** wherein a first intermediate member **(col. 10, line 22: "metal members 5")** and a second intermediate member **(col. 10, line 32: "first resin 9")** made of a material having a lower heat conductivity than said first intermediate member **(it is implicit that resin 9 has lower heat conductivity than metal member 5)** are provided under the lower surface of said semiconductor chip **(1)** and between the first base material **(19)** and said semiconductor chip **(1)**. Tamaki also teaches wherein the first and second intermediate members **(5 and 9, Fig. 1)** touch the lower surface of the semiconductor chip **(1)** and the first base material **(19)**; and wherein an area where the second intermediate member **(9)** touches the lower surface of the semiconductor chip **(1)** is larger than an area where the first intermediate member **(5)** touches the lower surface of the semiconductor chip **(Fig. 1)**.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to incorporate the teachings of Tamaki into the device of Yanagisawa, to form a first and second intermediate member between the chip and base material in order to improve both the mechanical and electrical bonding between the chip and the first base material.

Regarding the limitation of "a wide band gap semiconductor," note that using wide band gap semiconductors to construct power semiconductor devices was well known and conventional in the semiconductor art at the time of the invention, and thus, is generally recognized as being within the level of ordinary skill in the art.

With respect to **claim 2, Yanagisawa and Tamaki** teach the semiconductor apparatus of claim 1, as set forth above. Regarding the limitation, “wherein said power semiconductor device has a region where a current passes at a current density of 50 A/cm^2 or more,” Applicant has not shown such a claimed range to be critical or yield unpredictable results, and thus, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. See *In re Aller*, 220 F.2d 454, 105 USPQ 233, 234 (CCPA 1955). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to form a power semiconductor device with a current density as claimed, because the prior art teaches a device substantially identical in structure and material, to that of Applicant’s claimed invention.

With respect to **claim 3, Yanagisawa** teaches wherein said encapsulating material is made of resin **(21, Fig. 2; ¶ [0042])** and said heat conducting member **(15)** is exposed from said encapsulating material **(21, Fig. 2)**.

With respect to **claim 15, Yanagisawa** teaches wherein another heat conducting member **(16, Fig. 2)** is in direct contact with the lower face of said semiconductor chip **(11)**.

With respect to **claim 19, Yanagisawa and Tamaki** teach the semiconductor apparatus of claim 1, as set forth above. Furthermore, SiC is a well known wide band gap semiconductor used to construct power semiconductor devices, and thus, is generally recognized as being within the level of ordinary skill in the art.

1. **Claims 1-4, 18 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Mamitsu et al. (US 6,703,707; hereinafter, Mamitsu)** in view of **Tamaki (US 6,157,080; cited above)**.

With respect to **claim 1, Mamitsu** teaches a semiconductor apparatus **(Fig. 36)** comprising:

a semiconductor chip **(501a, Fig. 36)** including a power semiconductor device **(col. 33, line 50)**;

a first base material **(504, Fig. 36)** made of an electrically conductive material **(col. 34, lines 26-27)** and electrically connected **(through bond members 502)** to a part of a lower surface **(505b)** of said semiconductor chip **(501a)**;

a heat conducting member **(503, Fig. 36)** coming in contact with a part of an upper surface **(505a)** of said semiconductor chip **(501a)** and releasing heat directly from said semiconductor chip **(col. 37, lines 41-52)**;

an encapsulating material **(514, Fig. 36)** for encapsulating said semiconductor chip **(501a)** and said heat conducting member **(503)**;

wherein the semiconductor apparatus further comprises a second base material **(509/510, Fig. 36)** made of a metal material **(col. 34, lines 45-46)** and connected to a part of said upper surface **(505a)** of said semiconductor chip **(501a)**,

wherein said power semiconductor device is a vertical element **(col. 33, lines 40-45)**,

wherein a part of said first base material **(504a, Fig. 27)** is extruded outside said encapsulating material **(514)** and works as a first external connection terminal **(col. 35, lines 5-10)**;

wherein a part of said second base material **(509, Fig. 36)** is extruded outside said encapsulating material **(514)** and works as a second external connection terminal,

wherein a first intermediate member **(502, Fig. 36)** made of an electrically conductive material **(col. 34, lines 27-29: solder)** and a second intermediate member **(514, Fig. 36)** made of a material **(col. 34, lines 64-66: resin)** having lower heat conductivity than said first intermediate member **(solder 502)** are provided between said first base material **(504)** and said semiconductor chip **(501a)**, and touch the lower surface of the semiconductor chip and the first base material **(Fig. 36)**; and

wherein the semiconductor chip **(501a, Fig. 36)** and the first base material **(504)** are electrically connected with each other through the first intermediate member **(502)**.

Thus, **Mamitsu** teaches all the limitations of the claim with the exception of disclosing:

wherein an area where the second intermediate member touches the lower surface of the semiconductor chip is larger than an area where the first intermediate member touches the lower surface of the semiconductor chip; and

wherein the power semiconductor device is constructed by using a wide band gap semiconductor.

However, **Tamaki** teaches a semiconductor device **(Fig. 1)** wherein a first intermediate member **(col. 10, line 22: "metal members 5")** and a second intermediate member **(col. 10, line 32: "first resin 9")** are provided under the lower surface of said semiconductor chip **(1)** and between the first base material **(19)** and said semiconductor chip **(1)**. Tamaki also teaches wherein the first and second intermediate members **(5 and 9, Fig. 1)** touch the lower surface of the semiconductor chip **(1)** and the first base material **(19)**, and an area where the second intermediate member **(9)** touches the lower surface of the semiconductor chip **(1)** is larger than an area where the first intermediate member **(5)** touches the lower surface of the semiconductor chip.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to incorporate the teachings of Tamaki into the device of Mamitsu, to form the first and second intermediate members between the chip and base material, as

taught by Tamaki, in order to improve both the mechanical and electrical bonding within the semiconductor apparatus.

Regarding the limitation of "a wide band gap semiconductor," note that using wide band gap semiconductors to construct power semiconductor devices was well known and conventional in the semiconductor art at the time of the invention, and thus, is generally recognized as being within the level of ordinary skill in the art.

With respect to **claim 2, Mamitsu and Tamaki** teach the semiconductor apparatus of claim 1, as set forth above. Regarding the limitation, "wherein said power semiconductor device has a region where a current passes at a current density of 50 A/cm^2 or more," Applicant has not shown such a claimed range to be critical or yield unpredictable results, and thus, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. See *In re Aller*, 220 F.2d 454, 105 USPQ 233, 234 (CCPA 1955). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to form a power semiconductor device with a current density as claimed, because the prior art teaches a device substantially identical in structure and material, to that of Applicant's claimed invention.

With respect to **claim 3, Mamitsu** teaches wherein said encapsulating material **(514, Fig. 36)** is made of a resin or glass **(col. 34, line 66)**, and said heat conducting member **(503)** is exposed from said encapsulating material **(Fig. 514)**.

With respect to **claim 4, Mamitsu** teaches wherein said apparatus further comprises a radiation fin **(col. 37, lines 41-52: "cooling member")** that is contact with

said heat conducting member **(503)** and is extruded outside said encapsulating material **(514, Fig. 36)**.

With respect to **claim 18, Mamitsu** teaches wherein said external connection terminal of said first base material **(504)** is configured to be mounted **(col. 33, lines 44-45)**. It is well known in the art that terminals are configured to be mounted on a print wiring board. Furthermore, note that limitation of "configured to be mounted on a print wiring board," is considered functional language. It has been held that an apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Schreiber,* 128 F.3d 1473, 1477-78, 44USPQ2d 1429, 1431-32 (Fed. Cir. 1997).

With respect to **claim 19, Mamitsu and Tamaki** teach the semiconductor apparatus of claim 1, as set forth above. Furthermore, SiC is a well known wide band gap semiconductor used to construct power semiconductor devices, and thus, is generally recognized as being within the level of ordinary skill in the art.

3. **Claim 17** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Mamitsu (US '707; cited above) and Tamaki ('080; cited above)**, as applied to claim 3 above, and further in view of **Wu et al. (US 6,590,281; hereinafter, Wu).**

With respect to **claim 17, Mamitsu** further discloses another semiconductor chip **(501b, Fig. 36)**, which is also connected to said first base material **(504)**. However, neither **Mamitsu** nor **Tamaki** teach wherein said another semiconductor is stacked on the first semiconductor chip.

However, **Wu** teaches a semiconductor apparatus wherein a semiconductor chip **(24, Fig. 4)** is stacked on another semiconductor chip **(25)**. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to combine the teaching of Wu, with the teachings of Mamitsu and Tamaki, to form a semiconductor apparatus wherein two semiconductor chips are stacked on top of each other, for the purpose of reducing the package size.

Response to Arguments

4. Applicant's arguments filed September 28, 2009, have been considered but are moot in view of new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is (571)272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K./
Examiner, Art Unit 2814

/Wael M Fahmy/
Supervisory Patent Examiner, Art Unit 2814